What is claimed is:

1. A memory device, comprising:

a memory array, including a plurality of memory locations divided into memory pages, where each memory location has a row address and a column address;

a row decoder connected to the memory array for selecting a row address in the memory array;

a column decoder connected to the memory array for selecting a column address in the memory array; and

a multi-sequence address generator for generating addresses, where the multi-sequence address generator has a burst mode and in burst mode generates one of two or more burst sequences of addresses according to received burst parameters, and where each sequence has an index indicating the separation between two addresses in the sequence.

2. The memory device of claim 1, where the memory array comprises two or more memory banks and one page can be active in each bank at one time.

3. The memory device of claim 2, where a second page can be activated while a first page is being accessed using a burst sequence.

4. The memory device of claim 1, where a row address indicates a page in the memory array, and a column address indicates a memory location within a page.

5. The memory device of claim 1, where the multi-sequence address generator supplies an address to the column decoder.

6. The memory device of claim 1, where the burst parameters include a starting address, an index parameter, and a burst length.

7. The memory device of claim 6, where the index parameter is a value to be added to an address to create a burst sequence.

8. The memory device of claim 6, where the index parameter is a code to select one of two or more indexes provided by the multi-sequence address generator.

9. The memory device of claim 1, where one sequence has an index of one.

10. The memory device of claim 1, where one sequence has an index of eight.

11. The memory device of claim 1, where one sequence has an index of sixteen.

12. A memory device, comprising:

a plurality of memory locations, where each memory location has an address; and

an address generator, where the address generator generates two or more sequences of addresses by incrementing a starting address by an index corresponding to the sequence to be generated.

13. A data system, comprising:

a data source providing data in a first data order;

a data destination receiving data in a second data order; and

a scan converter system including a multi-sequence memory device, where the multi-sequence memory device includes:

a memory array, including a plurality of memory locations divided into memory pages, where each memory location has a row address and a column address;

a multi-sequence address generator for generating addresses, where the multi-sequence address generator has a burst mode and in burst mode generates one of two burst sequences of addresses according to received burst parameters, each sequence has an index indicating the separation between two addresses in the

sequence, and each of the two burst sequences corresponds to a respective data order.

14. A method of generating a burst sequence of addresses, comprising:

receiving a burst request, including a starting address, an index parameter, and a burst length, where the index parameter indicates an index; and

generating a burst sequence of one or more addresses having a number of addresses equal to the burst length, where the first address is the starting address and any additional addresses are generated by adding the index to the previous address in the burst sequence.

15. The method of claim 14, where the index parameter is a code to select one of two or more indexes.

16. The method of claim 14, where the index parameter is an index.